TouchStone

The Characterization Engine

interra systems

Automating Memory Charactertizaion

Manual methods of performing memory characterization are time consuming and error prone. More so, manual checks for errors and multiple regeneration of memory behavior requirement affect productivity and time-to-market. Designers need a tool that is capable of automating the process of characterization and verifying the memory based on required memory behavior.

Interra's Touchstone automates memory characterization to rapidly provide accurate timing and power models for simulation, verification, and synthesis. Touchstone enables designers to quickly and accurately validate memory architectures that are high in performance and low in power consumption.

Easily programmable, Touchstone comes as a user-friendly platform to describe and characterize memories. Further, Touchstone can be easily integrated with MC2, Interra's comprehensive memory development platform.

Touchstone is available on Linux platform.

Key Advantages

Automates memory design and reduces manual effort in memory development

Is independent of memory type

Supports characterization instructions at a higher level of abstraction

Supports parallel simulations

Supports a modular and hierarchical mechanism for specifying memory operations for characterization

Supports multiple simulators

Can be easily integrated into the Design Flows and modified for user-specific requirements

Comes with field-proven quality and tested processes that offer predictable quality

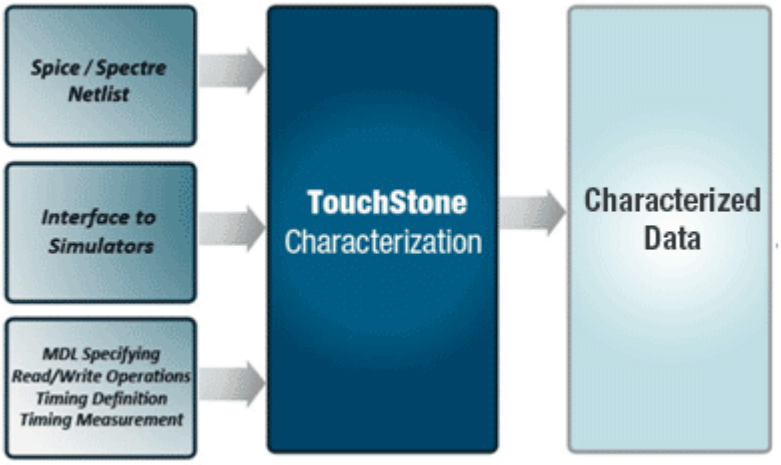
Can be easily integrated with MC2 to provide a complete Memory Development Environment

Salient Features

- Performs Timing characterization and Power characterization

  Setup Time Calculation, Hold Time Calculation, Bisection Method, Calculation based on Signal arrival time, Delay calculation, Transition Time calculation, Width Calculation, Cycle Time Calculation

  Static power, Dynamic power, leakage power, Power calculation based on custom mathematical expression
- Calculates capacitances, Rise and fall Currents
- Characterizes multiple PVT corners, multiple slew-load pairs, and multiple configurations using single instruction file
- Measures setup, hold, delay, power, etc., for various slew load pairs of two or more participating signals
- Interfaces with third party simulators: HSPICE, HSIM, and SPECTRE
- Results can be generated in various formats: Tabular format (log file), raw data file format, Synopsys liberty format, or any custom format
- Functional Verification
- On the fly glitch calculation
- Viewer for showing characterization vectors



MC2: Memory Development platform from Interra Systems.
MDL: A proprietary language from Interra System to define tiling, netlisting, and characterization vectors

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